Bit Cell Stability Testing using an Encoded 8-Positioner SEM Nanoprobing System

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Abstract. Non-visual fails have become an ever present hurdle in the IC industry. Eight probe contact nano probing on SRAM bit cells allows characterization of the bit cell's performance as a whole. This paper explains how nano probing on an individual bit cell, consisting of six transistors, can be performed on a die. Electrical connection is made with eight individual probes at the Metal-1 layer to test the bit cell for both stability and writing problems. Stability tests are performed at varying voltages to achieve many different examinations of the bit cell. In this experiment, voltages applied to the bit cell were: 1.5V, 1.2V, 1.0V, 0.8V, 0.6V, 0.4V and 0.2V.

Keywords: Nano Probing, SRAM, Bit Cell, Cell Stability Test.

INTRODUCTION

As the design scale for integrated circuits (ICs) decreases, failure analysis (FA) of transistor devices 65nm and below is becoming more challenging. Addressing these new challenges, scanning electron microscope (SEM) based nano probing has become a widely accepted technique to isolate parametric, or non-visual, fails. Recently, the ability to nano probe individual in-die transistors at the contact level, with four metallic ultra sharp probes, has given back to FA labs the edge that was lost when scale down reached the limits of optical based probing.

Individual transistors in SRAM, DRAM, flash RAM and logic devices are now routinely nano probed at the tungsten contact level with SEM based nano prober systems equipped with four probes. With a nano prober system equipped with eight probes, multi device tests can now be achieved. For example, with six and eight probes respectively, butterfly curves and the bit cell stability tests can be conducted on a 6T SRAM bit cell at the Metal-1 layer. When conducted at the Metal-1 layer, where transistors are connected to form the complete bit circuit, results from these tests provide a better measurement of how the transistors are working together as a bit cell.

In this paper, we demonstrate 8 -point contact nano probing of an SRAM bit cell found in an off-the-shelf, 65nm node technology IC.

EXPERIMENTAL APPARATUS AND PROBING TECHNIQUES

THE SAMPLE

An Intel™ E6600 Dual Core Processor was purchased from a mass market retail electronics supply store. Chip depackaging and deprocessing was done at Microtech Analytical Labs. After careful depackaging, the chip was mechanically polished with diamond grit down to the Metal-2 layer. Next, the diamond mechanical polish media was thoroughly cleaned off, then deprocessing continued with colloidal silica chemical mechanical polish (CMP) media until the copper Metal-1 layer was reached. Finally, the polish media was cleaned away and the chip was mounted on an aluminum SEM specimen holder.

Nano Probing System Description

The Zyvex nProber™ is a fully integrated nanoprobing system consisting of a field emission gun (FEG) SEM, an 8-probe and sample nano positioning platform, computer aided design (CAD) navigation, a Keithley 4200 parametric analyzer, a sample exchange load lock and an *in-situ* ion source sample and probe cleaning unit. The motions of each of the 8-probe positioners are closed loop encoded to 1 micron

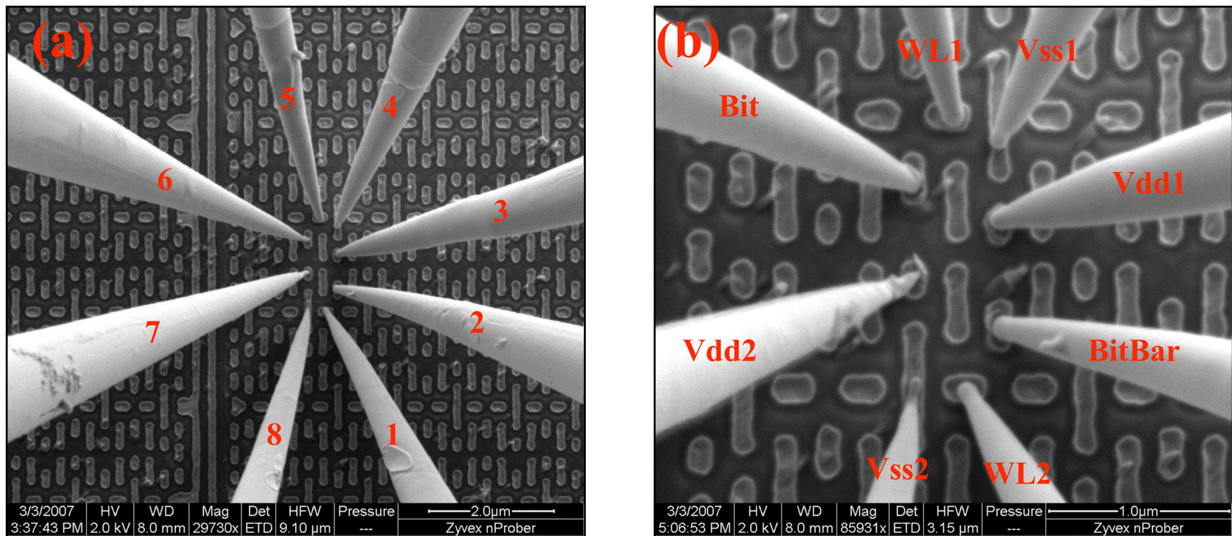

FIGURE 1. *SEM images of the SRAM bit cell DUT with eight tungsten probes in contact with the copper Metal-1 connections at (a) 30,000x magnification and (b) 85,000x magnification.*

resolution, with a range of motion of 12mm, in the three Cartesian (xyz) axes. For precise nano positioning, the positioners have an additional "fine mode" of motion with a resolution of 5nm. This combination of range of motion and resolution allows each positioner to place its probe tip within a $12mm^3$ volume with 5nm resolution.

The nProber's center stage sits at the center of the prober unit and below the probe positioners. Its range of motion (28mm x 28mm x 13mm) is larger than the eight positioners to allow the positioning of a 1cm diameter sample as well as to allow sample exchange. The center stage also has closed loop encoding to 5nm resolution in all three xyz axes. Coupled with the CAD navigation system, the Center Stage will move to anywhere the CAD system points. Nanoscale step-and-repeat measurements on identical devices can be achieved, which allows the new ability to determine the performance of devices as their location moves away from a failure site.

The nProber uses tri-axial cables to connect the parametric analyzer through a vacuum interface to each probe. This feature allows the system to have low electrical leakage and noise to below 200fA, so that low level I_{off} and critical leakage measurements on SRAM transistors can be achieved.

Nano Probing Technique

The nProber was loaded with eight Zyvex probes prepared using a proprietary process and bent to a 45 degree angle. To avoid buildup of hydrocarbon contamination on the chip during SEM imaging, the chip was decontaminated with a down stream asher integrated into the nProber's sample exchange system. This process is a well-known solution to the "black box" problem that forms on samples during SEM imaging. [1] Once the chip was decontaminated of hydrocarbons and transferred from the sample exchange system onto the nano probing stage (located in the SEM sample chamber vacuum), the chip was ion sputter cleaned with the integrated 5 keV argon ion source. This system removed copper oxide from the Metal-1 copper traces by using a 2mm diameter argon ion beam with a beam energy of 5 keV. Hydrocarbon decontamination and argon ion sputter cleaning are important steps that greatly reduce the probe tip to sample electrical contact resistance. These preparation steps are carried out *in-situ*, and as a result, the chip will stay free of contamination and oxide for many hours of nano probing.

Once the sample and probes were ready for probing, the operator positioned the probe tips just above the chip's surface with a few button clicks on the graphical user interface (GUI). After the sample and probes were at the optimal arrangement for landing, the CAD navigation system was used to do a 3-point alignment of the center stage to the chip layout. This was accomplished by selecting three arbitrary points on the layout and moving the sample stage, by point-and-click method, to each point to set the alignment. Usually, the three points are chosen to be within the bank that contains the bit intended for probing, while also being as far from each other as possible. This ensures that the layout in the navigation system matches the chip layout on the sample stage,

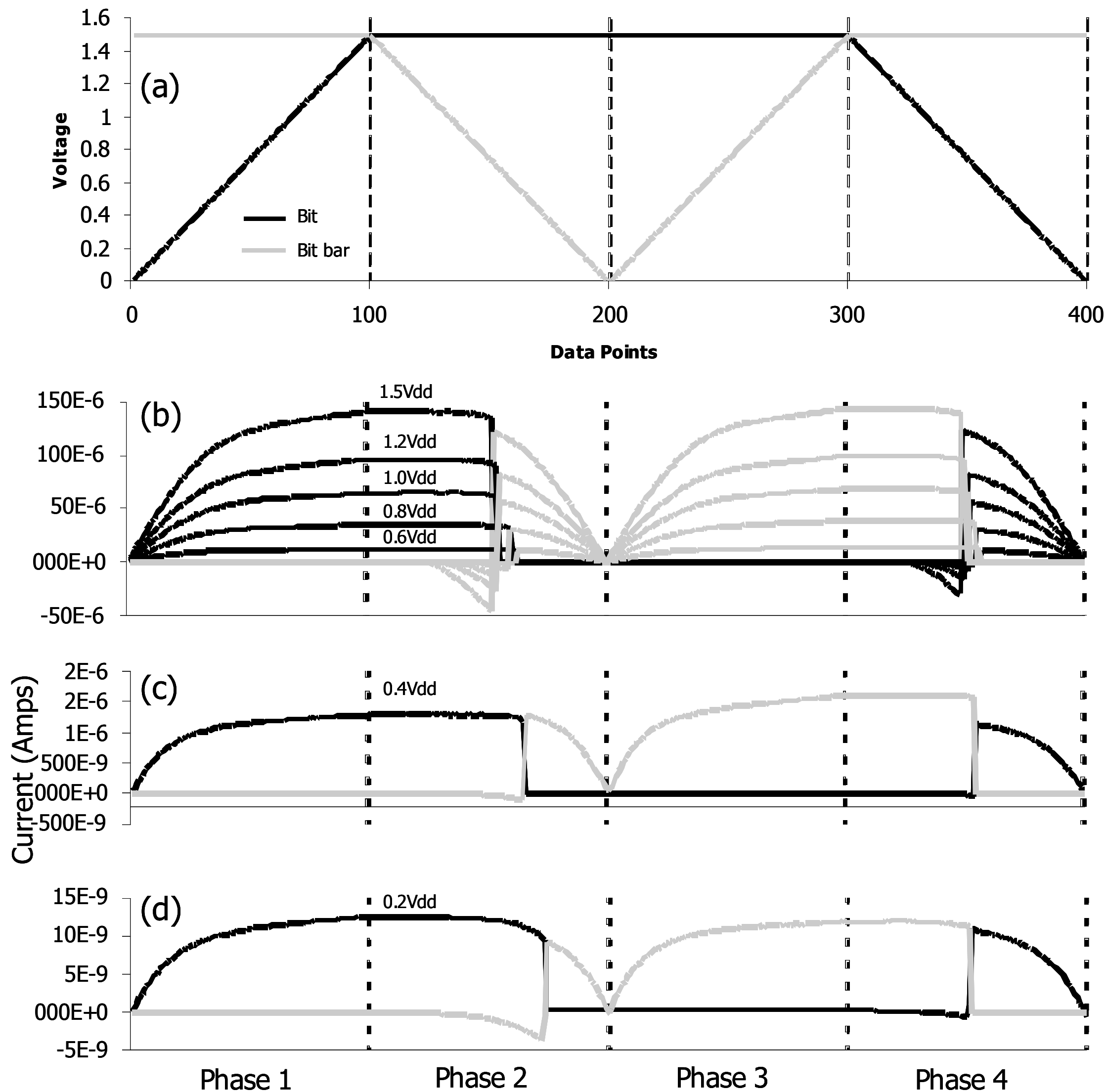

FIGURE 2. *(a) List sweep voltage plots for Bit and Bitbar of a bit cell. (b)-(d) Bit cell stability tests of a 65nm technology in die SRAM. Bit and Bitbar current was collected with Vdd settings from (b) 1.5 volts to 0.6 volts giving high current values and (c) 0.4 volts giving medium current values and (d) 0.2 volts giving low current values.*

including any small amount of sample rotation. By entering the coordinates of the targeted SRAM bit into the CAD interface, the center stage was automatically moved to the position of the intended bit. As a result, no time consuming row and column counting (which can produce errors) was needed to locate the area intended for probing.

The next step in the process flow, was to land the eight probes needed for bit cell probing on the sample's surface. Each probe was landed by selecting it individually on the joystick keypad and starting the auto approach function. The selected probe lowered slowly toward the chip's surface until the operator detected the moment of contact by observing a small tip deflection. At that moment, the operator deflected the joystick, signaling the positioner immediately to stop moving down, and then to lift the probe up off of the surface by a few microns. This auto approach function was repeated until all eight probes were just a few microns above the chip's surface. By using the joystick, final adjustment of the probe tips' locations and the final electrical connections to the intended bit cell contacts were made (as shown in Figure 1). Landing the probes on the soft Metal-1 traces can damage the traces if the operator allows the probes to press with too great a force. However, the contact

force can be managed by the operator so that surface scarring or smearing of the copper is minimized. Managing a system with eight probes could be a difficult task, but with closed loop control and point-and-click commands, the demands placed on the operator are reduced.

With nanoscale surfaces, mechanical contact does not always equate to electrical contact. Therefore, when nano probing, electrical connection should always be verified before collecting any valid data. A current *vs.* time or I *vs.* t procedure was used to verify and maximize the electrical connection between the probe tips and the Metal-1 traces. In the I *vs.* t procedure, probes are voltage biased with fixed values so that either the bit (or some part of the bit) is powered while the current is plotted *vs.* time. The operator then made small adjustments to the probes, including lifting up and setting down each probe, until the observed device output current was either maximized or reached the expected level. Then the I *vs.* t test was terminated by setting the probes to zero bias. This I *vs.* t procedure can be repeated for different parts of the bit until the operator verifies that all connections are optimal. Finally the operator started the bit cell stability test.

RESULTS AND DISCUSSION

The data was collected through the Zyvex DC Measurement interface which communicates with the Keithley 4200 parametric analyzer. The battery of test parameters that were used for bit cell probing were pre programmed into a table called a list sweep. With this type of test, potentially any arbitrary set points for current or voltage can be loaded into the table called the “list”. In the case of the bit cell stability test described here, the list contained sweeping voltage and holding voltage (depending on what stage of the test was being conducted). With eight probes making the connections to a single bit and the list sweep generating the waveform needed to program and read the bit, the bit cell stability test can be performed. The Bit and Bitbar connections were swept in a way that would read and program the bit while the Vdd and Vss connections independently powered the bit and the wordline connections were held at Vdd. Shown in Figure 2(a), the bit cell stability test has four phases; Phase 1 initializes the data in the cell to a logical 0, while measuring the read current vs. bitline voltage as bitline ramps up to Vdd. If the cell flips in this phase, the cell is unstable. Phase 2 writes the opposite data. When the cell writes, a reversal in currents is observed. Stability problems are indicated if the cell writes at voltages close to Vdd. If the cell writes at voltages close to 0V, then the cell has write ability problems; if the cell never flips, it is not writeable. In Phase 3, the cell should contain data equal to a Logical 1. While measuring the read current vs. Bitbar voltage, Bitbar ramps up to Vdd. If the cell flips in this phase, the cell is unstable. Phase 4 is similar to Phase 2, except Bit and Bitbar are swapped.

Figure 2b, 2c and 2d shows a series of 7-bit cell tests that were measured by additionally stepping the voltage applied to Vdd from 1.5V to 0.2V for each test, spanning Phases 1 through 4. More evident in Figures 2c and 2d, the bit flips later as the Vdd voltage is lowered. The current compliance, or limit for the bit connections, was set to 500µA. Before and during data acquisition, the microscope’s scanning beam was blanked to minimize any charge-induced influence.

After all of the parametric data was collected from the DUT, the operator pressed the “Disengage Probes” button on the GUI. This lifted each of the probe tips 3 microns above the chip surface. At this point, the operator could index the Center Stage to the next identical bit over as a step-and-repeat operation. Once the probing was done, the “Stop Probing” button on the GUI was pushed by the operator and the probes lifted and pulled back to neutral positions. The Center Stage dropped 100 microns to be in a safe but near position if probing was to continue at a later time. Finally, the “Sample Extraction” command was executed by the operator through the GUI, lowering the sample even further and allowing it to be extracted through the sample exchange system.

SUMMARY

The bit cell stability tests allow semiconductor SRAM designers and manufacturing failure analysis engineers to see the voltage at which the bit cell flips state. The test result indicates how stable or writeable the cell is, by observing the voltage when the read currents reverse.

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