Measuring Static Noise Margin of 65nm Node SRAMS using a 7-Positioner SEM Nanoprobing Technique

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Abstract. Non-visual fails have become an ever present complication in the IC industry. Nano probing SRAM bit cells at the inverter level allows the cell to be tested and static noise margin (SNM) to be measured. This paper explains how nano probing of a 65nm technology 6 transistor bit cell was performed and SNM dependence on supply voltage was measured for both hold and read modes. Connection to the bit cell was made at the Metal-1 layer with seven nano probes to collect the voltage transfer curves (VTCs) of the two inverters of the cell. In this experiment, each inverter was tested by varying Vdd voltage from 1.5, 1.2, 1.0, 0.8, 0.6, 0.4 and 0.2V while collecting the VTC. The two VTCs of the cell are plotted to produce the cell's butterfly curve from which the SNM is found graphically for each setting of Vdd.

Keywords. Nano probing, SRAM, Bit Cell, Butterfly Curves, Voltage Transfer curves, VTC, Static Noise Margin, SNM, 65nm Technology

INTRODUCTION

In this paper we report, for the first time, a technique for measuring the static noise margin (SNM) of in die 6T SRAM bit cells using an SEM based nanoprobing system. The SNM of a bit cell quantifies the amount of electrical noise that is required, at the cell's internal nodes, to flip the cell's contents [1,2]. This information is vital to the engineering cycle to produce faster and more efficient SRAM designs. With the aid of SEM-based nanoprobing systems that are equipped with eight or more probes, measurements such as SNM and bit cell stability are now possible on in-die SRAM transistors.

EXPERIMENTAL

The SRAMs measured for this paper were based on the 65nm IC process and were obtained by purchasing an off-the-shelf microprocessor. An Intel™ E6600 Dual Core Processor was purchased from a mass market retail electronics supply store. The depackaging and deprocessing of the chip was done at MAL [3]. After careful depackaging, the chip was mechanically polished with diamond grit down to the Metal-2 layer. After thoroughly cleaning off the diamond mechanical polish media, the deprocessing resumed with a colloidal silica chemical mechanical polish (CMP) media until the copper Metal-1 layer was reached. At this level, interconnectivity of the SRAM transistors was sufficient to allow SNM measurements of an isolated SRAM bit cell. The chip was then cleaned of the polish media and mounted on an aluminum SEM specimen holder with vacuum compatible, single sided, adhesive, copper tape.

A Zyvex nProber™ System was used for all imaging and data collection for this paper. It is a fully integrated system consisting of a field emission gun (FEG) SEM, eight probe and sample nano positioning platform, computer aided design (CAD) navigation, Keithley 4200-SCS parametric analyzer with 8 SMU/preamp, a sample exchange load lock and an *in-situ* sample and probe cleaning system. The prober uses tri-axial cables to connect the analyzer through a vacuum interface to each probe. This feature allows the system to have low electrical leakage and noise (below 200fA) so that low level Ioff and critical leakage measurements on SRAM transistors can be achieved. The prober was loaded with eight Zyvex NanoEffector® probes prepared using a proprietary Zyvex process and bent to a 45-degree angle.

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To avoid buildup of hydrocarbon contamination on the chip during SEM imaging, the chip was decontaminated with a down stream asher that is integrated into the nProber's sample exchange system. This process is a well-known solution [4] to the "black box" problem that forms on samples during SEM imaging. Once the chip was decontaminated of hydrocarbons and transferred from the sample exchange system onto the nano probing stage located in the SEM sample vacuum chamber, the chip was ion sputter cleaned with an integrated 5 keV argon ion source. This system removed copper oxide from the Metal-1 copper traces by using a 2mm diameter argon ion beam with a beam energy of 5 keV. These two steps, hydrocarbon decontamination and argon ion sputter cleaning, are important tasks that greatly reduce the probe tip to sample electrical contact resistance. These preparation steps were carried out *in-situ* and, as a result, the chip stayed contamination and oxide free for many hours of nano probing.

RESULTS AND DISCUSSION

Figure 1a shows the schematic of the bit cell at Metal-1 and the large black dots indicate the nano probe tip/sample contact locations for the two inverters of the bit cell. The SEM photo in Figure 1b shows six nano probes used to supply and measure voltage on one of the two inverters of a bit cell. Not shown is a seventh nano probe placed on the well connection that is out of the view of Figure 1b. Had this bit cell been based on silicon on insulator technology, the seventh probe would not have been necessary.

The voltage transfer curves (VTCs) of inverter 1 were collected by supplying the needed fixed voltage to the Vdd, Vss, Wordline, and Bitline and sweeping voltage on the CL connection while measuring voltage on the CH connection. The VTCs of inverter 2 were collected in the same manner with the exception that the bias of the CH connection was swept and voltage was measured at the CL connection. Data was collected for both "Read" and "Hold" conditions whereas the WL connection was held at Vdd for "Read" and 0.0 volts for "Hold."

The butterfly curves of Figure 2 were created by taking the VTCs of inverter 1 and inverting the curves and plotting them with the VTCs of inverter 2. Figure 2 shows the butterfly curves along with the graphically determined SNM for "Read" and "Hold" with the Vdd held at 1.0 volts. The square having the longest diagonal between the VTCs of the two inverters gives the SNM by the length of the side of the square. If the butterfly curve is asymmetric, as illustrated in Figure 2a, by having a small and a large square in the two openings of the curve, then the smaller of the two squares is used for determining the SNM [1]. Figure 2a shows that the SNM is lower during the Read function and this is because the VTC is degraded by the voltage divider across the pass gate transistor and the drive transistor.

By collecting the SNM values for the bit under test and varying the Vdd from 1.5V to 0.2V we can determine the bit's dependence on supply voltage and its ability to retain data. If the supply voltage is lowered so that the SNM is just greater than 0.0 then that point is the data retention voltage (DRV). Other factors can affect the SNM such as temperature and process variation [2].

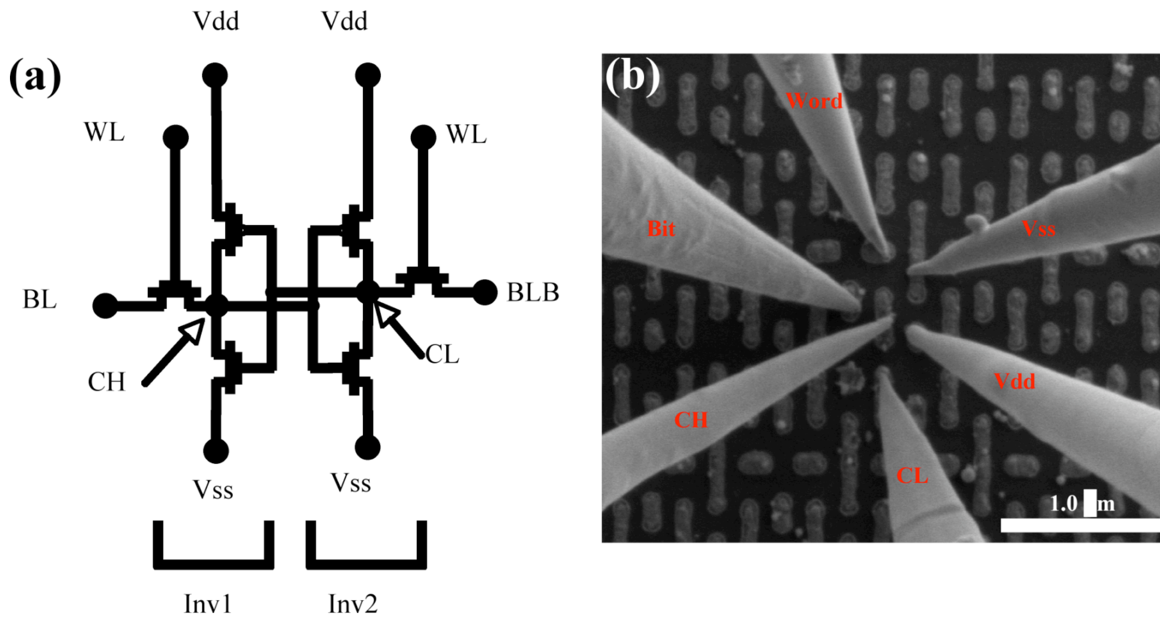

FIGURE 1. Schematic for the 6T bit cell at Metal-1 showing the probe contact locations (a). SEM image taken at 1keV of the nano probes in contact with inverter 1 at the copper Metal-1 layer (b).

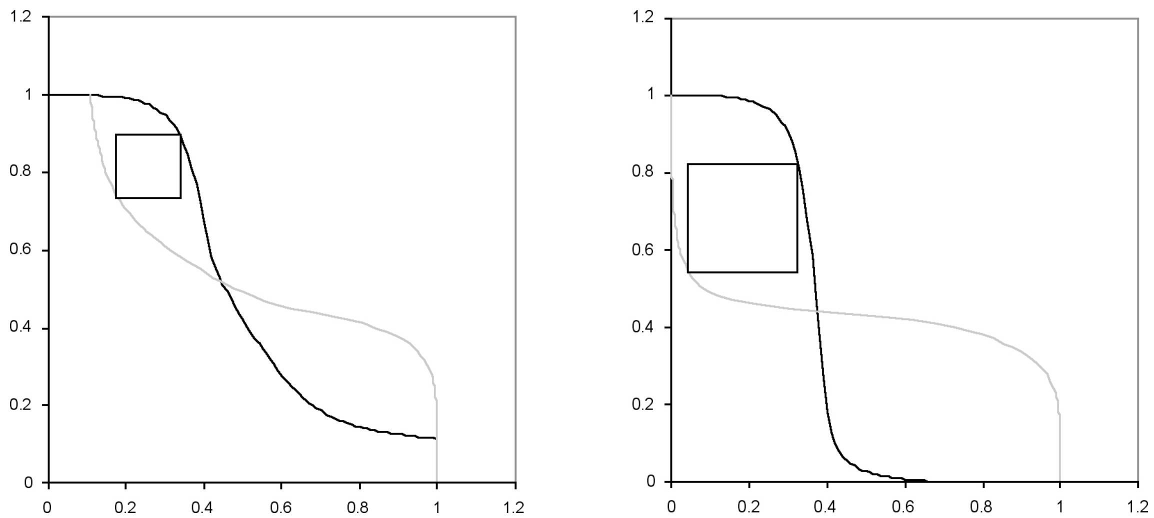

FIGURE 2. Butterfly plots of a 65nm node SRAM bit cell in read (a) and hold conditions (b).

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CONCLUSIONS

Individual transistors in SRAM, DRAM, flash RAM and logic devices are now routinely nano probed at the tungsten contact level with SEM based nano prober systems. With a nano prober system fitted with seven probes or more, the next level of testing can now be conducted. SNM is an important metric in determining the stability of 6T SRAM designs and their dependency on supply voltage and other factors. With SEM based nanoprobing, SNM can be measured on in-die bit cells.

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