Capacitance-Voltage Test using a SEM Nanoprober

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Abstract. The move from one technology node to the next, with the associated transistor geometries shrink, has significantly increased the occurrence of SRAM bit cell errors. Advanced failure analysis labs have employed scanning electron microscope (SEM) based probing systems to isolate individual failed transistors using the Vt curves and Id-Vd family of curves. However, the bit cell errors caused by interface trapped charges and doping related issues may not be thoroughly analyzed using these standard probing electrical tests. Hence, capacitance-voltage (C-V) measurements that are capable of studying oxide layers, interface traps, and charge carrier densities, are considered an appropriate tool to evaluate these conditions. In this communication, we demonstrate C-V testing on gate oxide of individual transistors from the SRAM of an Intel™ 45nm microprocessor using a Zyvex nanoprobing system and Keithley 4200 parametric analyzer fitted with the C-V option.

INTRODUCTION

Advanced microprocessors have SRAM memory cache on the chip which takes up roughly half of its total area. As device technology advances, the occurrence of bitcell errors has rapidly increased. Most of these bitcell errors occur when one of the six transistors which make up the 6T-SRAM bitcell fails to function properly resulting in bitcell instability. Since the transistors in an SRAM bitcell are hard wired together at the Metal 1 layer, these transistors must be exposed at the transistor contact level and addressed individually using a nanoprobing system. To test these transistors individually, SEM nanoprobers have been widely used by device failure analysis labs because they are capable of making electrical connection with the individual transistors of the SRAM bitcell which has been deprocessed to the contact level [1-6]. These nanoprobers typically have four or more independent probes and operate inside an SEM.

When defects are detected in a bit cell, an SEM nanoprober is used to evaluate the failed and near by reference transistors by obtaining and comparing their characteristics, such as the Threshold Voltage (Vt) Curves and Id-Vd Family Curves. However, failures caused by interface trapped charges or doping problems are more difficult to analyze and often DC transistor characterization is insufficient. Therefore, in order to evaluate such parametric failures, an alternative analytical method should be sought. Capacitance-voltage (C-V) measurement is considered to be a feasible analytical technique since C-V characterization is a conventional technique which has been used in conjunction with optical probing systems to evaluate the oxide layer thickness and charge carrier density in larger scale semiconductor devices [7]. Therefore, it is believed that C-V characterization will provide a wealth of similar information in nano-scale analysis. In this paper, we report the C-V results obtained from an Intel™ 45nm node 6T-SRAM bit cell characterized using a Zyvex sProber and Keithley 4200-CVU unit.

SAMPLE PREPARATION AND MEASUREMENT SYSTEMS

Sample

An Intel™ Penryn dual core 45nm technology node processor was used for this evaluation. This device was purchased from a local retail store and depackaged carefully. The chip was deprocessed by chemical and mechanical polishing using nitric acid and colloidal silica. Once the transistor contact layer was exposed, the sample was etched in 1% hydrofluoric acid and rinsed thoroughly with deionized water and isopropyl alcohol. Finally, the sample was dried by blowing with nitrogen gas and placed on an aluminum SEM sample stub with electrically conductive copper-nickel tape.

Measurement System Details

A Zyvex SEM nanoprober system consisting of a four positioner nanoprober, an anti-contamination system, a Keithley 4200 parametric analyzer, and

Zyvex software that manages all the components was used to conduct the C-V testing. The nanoprober system used had 12mm of travel with better than 5nm resolution in the x, y, and z axis. The sample was mounted on the sample stage which moves independent of the probe motion in the z-direction with 13mm of travel. The nanoprober is designed for quick installation and removal in the SEM. The SEM used was a LEO 1530 Schotky field emission microscope and all of the images were collected using the 30 micron aperture and the beam energy setting of 1keV.

The Keithley 4200 was upgraded with the 4200-CVU package, an advanced state-of-the-art C-V unit that provides a complete C-V solution. The Keithley 4200-CVU measures AC impedance of the device under test (DUT) by sourcing an AC voltage across the device and measuring the resulting AC current and phase. The capacitive impedance was calculated based on the measured impedance and phase; the capacitance was obtained from the capacitive impedance and the test frequency (1).

$$C_{DUT} = I_{DUT} \Big/ 2\pi f V_{AC} \tag{1}$$

The Keithley 4200-CVU was configured with two source lines and two sense lines. The source lines provide DC and/or AC voltage to the gate and/or drain contacts while the two sense lines measure the capacitance of the device with accuracy better than 0.1 femto-Farad. The force line sweeps a DC voltage while an AC voltage with fixed frequency between 10kHz and 10MHz is applied. The AC voltage can be applied through the same force line as the DC voltage or the AC voltage can be applied through the other force line. The capacitance between the gate and the drain of the transistor is measured by sweeping the gate with a DC voltage as a fixed AC voltage is applied to either the gate or the drain contact.

The equivalent oxide thickness (EOT) and the gate oxide thickness are determined from the measured capacitance and known gate area and dielectric constant using the following relationship (2).

$$C = \kappa \frac{A}{d} \tag{2}$$

Where κ is the dielectric constant of the insulator, A is the area of the capacitor, and d is the separation of the two plates [8].

SYSTEM SET-UP AND OPERATION

The prober was loaded with four Zyvex probes bent to a 45 degree angle and prepared using a proprietary Zyvex process. The entire SEM chamber and prober head unit including the sample chip was decontaminated for a few minutes with the Zyvex Optimizer anti-contamination system which removes hydrocarbons before probing to avoid buildup of carbon contamination on the chip during SEM imaging [9].

Once the sample and probes were ready for probing, the probe tips were positioned above the area of interest, and the sample stage was lifted up to the probe tips just short of touching. Two probes with radii better than 50nm, were landed on the appropriate contacts and C-V measurements were taken. More detailed explanation for probing can be found elsewhere [10]. During data acquisition, the microscope's scanning beam was blanked to minimize any charge-induced influence.

All data were acquired through the Keithley 4200-CVU parametric analyzer using the KITE interface via a virtual network computing (VNC) on the Zyvex PC. The Keithley

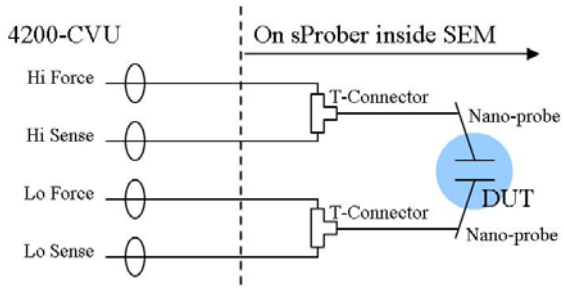

***FIGURE 1**. System setup*

4200 unit was connected to the probes via special low noise cables and a SEM feed-thru. Each CVU source line was teed with a CVU sense line on the prober head unit in order to have two source-sense pairs very close to the sample, thus, only two probes were used to collect the data (Figure 1). This was done to eliminate the need of placing 4 probe tips on the small contacts of the DUT. All four cable shields were also tied to have a common ground at the prober head unit. This configuration helps minimize stray capacitance and ground loops when the C-V measurement is carried out. It is important to connect the shields of the coaxial cables together as close as possible to the probe tips to reduce the loop area of the shields, which minimizes the cable inductance. If the shields are not connected together, large offsets may occur. Also, larger error is expected at higher frequency.

MEASUREMENT AND RESULTS

Measurement Parameters and Correction Factors

In the Keithley KITE interface, the pre-programmed C-V interactive test module was used for all of the measurements. Table 1 shows all the parameters used for the test. A frequency of 1 MHz and an AC voltage of 100mV RMS were used for all tests reported in this communication; however, using other lower frequency values could yield comparable results.

Before the data acquisition began, measurement corrections were performed according to Keithley's C-V guidelines [11]. This was done soon after touching down on the sample surface and lifting up to park the probes less than 10µ meters above the DUT contacts. Short correction, open correction, load correction, and cable length compensation methods are all available to improve the accuracy of the results. Devices with large impedance and small capacitance require an open correction. The cable length compensation and load correction should be done regardless of the device impedance.

The open correction was carried out while the probe tips were just above the contacts, thus, the connection was open and the baseline capacitance was measured. The baseline capacitance was automatically taken into account while the actual measurement was performed. The load correction and the cable length compensation correct the gain error and the phase shift, respectively. The gain error varies depending on the amount of capacitance being measured. A form of a load correction is to connect and measure a known standard load and calculate the ratio to make a measurement match the known load. One limitation of load correction is that it works best when the load is close to the value of the device intended to measure and in the case of this paper there was no known load available.

The cable length compensation corrects the phase shift occurring due to the time taken for the AC signal to travel through the cables. Therefore, higher phase shift is observed at higher frequency. It is also important to use the cables, which are provided and/or tested by Keithley, because the signal propagation speed varies depending on the cables. Equation (3) shows the relationship between the final corrected device impedance and all the corrections that are carried out before the test.

TABLE 1. List of Parameters

DC Voltage	Sweep -1.2 to +1.2
AC Voltage	100mV RMS
Frequency	1 MHz
Sweep Delay	2 seconds
Hold Time	5 seconds

$$Z_{corrected} = \frac{1}{\frac{1}{\left(Z_{msd} / LC_{msd}\right) - Z_S} - \frac{1}{Z_O}} \quad (3)$$

$Z_{corrected}$ = corrected final impedance
Z_{msd} = measured impedance
LC_{msd} = measured load correction
Z_S = measured short correction
Z_O = measured open correction

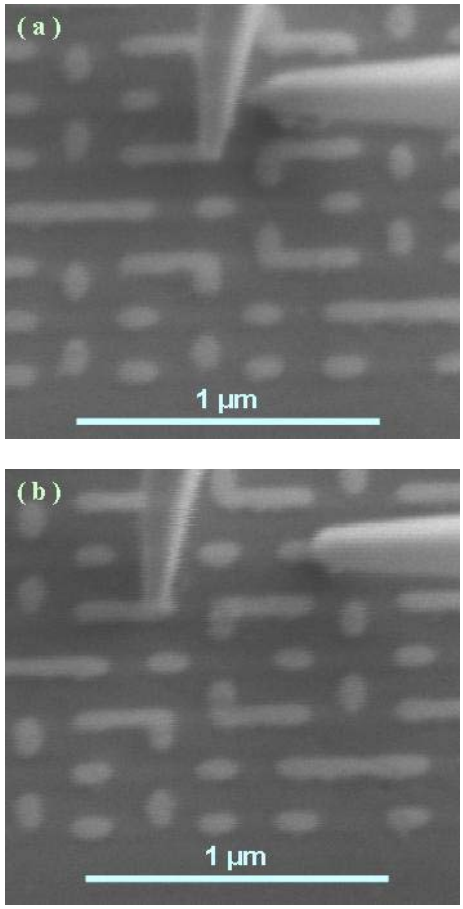

FIGURE 2. *Probes touching down on the contacts for C-V measurement, (a) PMOS and (b) NMOS of Intel™ 45nm SRAM at metal-0*

Results and Discussion

The C-V characterization of PMOS and NMOS transistors were measured while changing the AC and DC configuration. SEM images in Figure 2 show the tungsten probes making electrical connection with the 45nm PMOS and NMOS device contacts. Both the PMOS and NMOS devices were measured under a constant AC voltage applied while sweeping with a DC voltage. The following four different voltage configurations were used: DC and AC on gate, DC on gate and AC on drain, DC on drain and AC on gate and

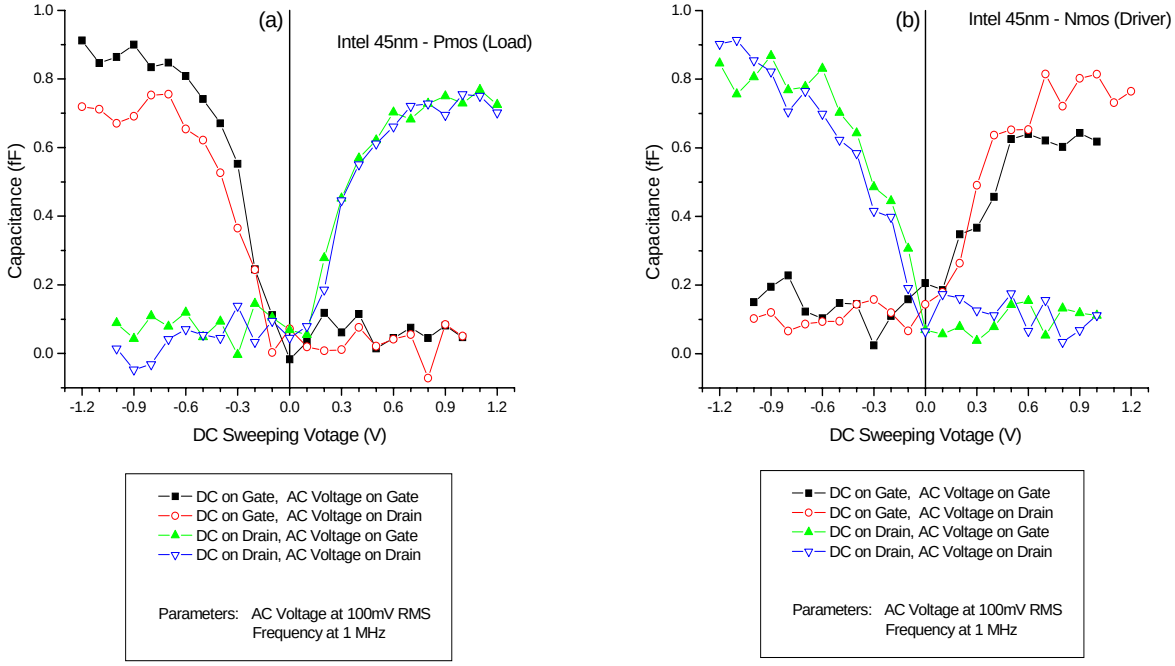

FIGURE 3. *Capacitance response of the gate of a) PMOS and b) NMOS while applying DC and AC voltages to gate and drain in the following configuration order: gate only, gate and drain, drain and gate, and drain only.*

both DC and AC on drain.

The plots in Figure 3 summarize the results. The overall noise level was a proximately 0.1fF while the maximum capacitance observed was about 1.0fF at an applied -1.2 volt DC. It is clear that the inversion and the accumulation switched places in the graphs as the applied DC voltage switched between gate and drain for both NMOS and PMOS. In other words, the capacitance is at an accumulation state when the device is on and conversely at an inversion state when the device is off. It is also clear that the capacitance curves of all configurations of the PMOS and NMOS are the mirror image of one another because the DC bias required for the devices to be turned on is roughly the same value but with an opposite sign and which also confirms the consistency of the measurements. All of the curves were collected from the inversion side and finished at the accumulation state.

SUMMARY

C-V characterization is a well-established technique for the study of inter-layer conditions and charge carrier densities of large-scale semiconductor devices using an optical probing system. Previously, the application of C-V measurement to nano-scale structures was thought to be a significant challenge. In this communication, successful gate capacitance measurements for transistors in an Intel™ 45nm Penryn Dual Core SRAM device were demonstrated at the contact level using a Zyvex nanoprobing system and a Keithley 4200-CVU.

For this report, only capacitances of working devices were measured. If, however, a soft failed device was tested, obvious characteristic changes would be expected which could lead us to understand the SRAM soft errors caused by interface trapped charges or doping issues. With a capacitor area and dielectric constant known, the oxide layer thickness can be derived based on the measured capacitance. Likewise, a charge carrier density or degradation of high-κ material can be determined. Understanding not only the characteristic but also the mechanism of the fails can increase the success rate of failure analysis, which also leads to the improvement of device reliability.

ACKNOWLEDGEMENT

We thank Keithley Instruments Engineers/Technologists in Ohio for lending us a CV card and also sharing valuable information.

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