EDFAAO (2009) 4:22-27 1537-0755/$19.00 ©ASM International®

Nanoprobing SRAM Bit Cells with High-Speed Pulses

Richard E. Stallcup II and Kanzan Inoue
Zyvex Instruments LLC
rstallcup@zyvex.com

Introduction

For a number of years, in-die SRAM transistors have been successfully probed using direct current (dc) nanoprobing to reveal faults for failure analysis and to verify in-die parametric performance for the engineering design loop.[1-5] These slow dc tests are needed for measuring subnanoampere gate and channel leakages. There has recently been interest in exploring the value of high-speed testing using a nanoprober. A well-known technique of high-speed pulse testing has been very useful for measuring the effects of self-heating in silicon-on-insulator devices, trapped charge in high-k dielectric material, and rapid testing that generates millions of waveforms per second.[6-8] All of these techniques were developed for use at the microscale. The reason these techniques have not been mainstream for nanoprobing is merely the perceived nanoscale barrier. Probing systems with high-speed capability are typically associated with the larger-scale optical-based microprobing systems. Historically, nanoprobing systems have been optimized for dc testing, but there is not a significant hurdle to their use in high-speed testing. This paper describes the use of a scanning electron microscope (SEM)-based nanoprobing system equipped with high-speed testing capability. The system, which is capable of 10 ns rise and fall times, is used to characterize in-die SRAM bit cells. A single high-speed test, taken at the bit cell level, determines the most likely failing transistor. This technique decreases fault localization time, and because the test is done at metallization layer 1, it decreases the possibility of deprocessing past the fail.

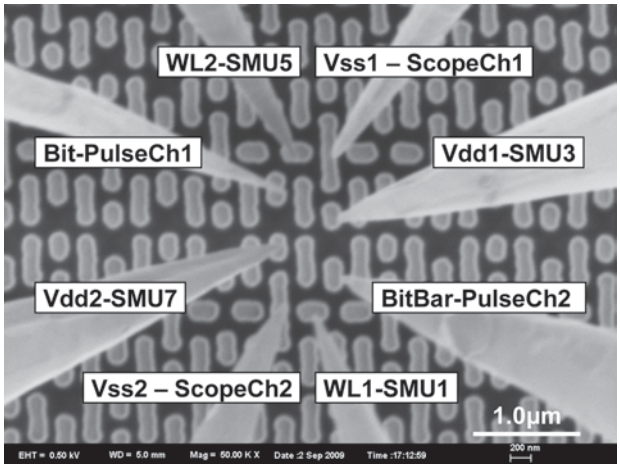

Fig. 1 *500 eV SEM image of eight nanoprobes contacting a 65 nm SRAM bit cell at the metal 1 layer*

System Setup

As shown in Fig. 1, pulse probing of in-die metal-1-level SRAM bit cells requires eight probe tips to power the bit, supply the pulse signals, and collect the bit's response or reaction to the pulse. Three pieces of integrated test equipment are used in conjunction with the Zyvex nProber System: a Keithley Instruments 4200 parametric analyzer, a Picosecond Pulse Labs two-channel 1.6 GHz pulse pattern generator, and a LeCroy 204xi four-channel 2 GHz bandwidth real-time digital oscilloscope with 50 Ω channels. The four probes supplying the dc power to the V_{dd} and word-line contacts were connected to individual source-measurement units (SMUs) on the parametric analyzer. The two probe tips supplying the fast pulse signals to the bit and bitbar contacts were connected to the two-channel 1.6 GHz pulse pattern generator. The fast pulse signal lines are 50 Ω terminated 25 mm back from the probe tip, inside the SEM vacuum. These signals are also connected to channels 1 and 2 of the oscilloscope via power divider tees, and these channels are used as pulse voltage monitors for bit and bitbar. The bit's reaction to the pulse pattern was collected on the oscilloscope through the probes connected to the two V_{ss} contacts. Thus, scope channels 3

and 4 were current monitors that were connected directly to the probes contacting V_{ss1} and V_{ss2}, respectively.

The sample was an off-the-shelf microprocessor based on 65 nm bulk technology. It was depackaged and deprocessed down to the copper metal 1 level, where the SRAM transistors of this technology are connected to form the cross-coupled inverters in each SRAM bit cell. In addition, the contacts of the bit cells at this level are isolated from neighboring cells. The SEM-based nanoprobing system provides the capability of placing tungsten probe tips with nanometer precision onto soft metal layers and individual tungsten contacts. The SEM provides a high-resolution video-rate image that facilitates locating the device and placing the probe tips in real time. The SEM is operated at 500 eV to ensure there is no transistor degradation. The nanoprober system is fully integrated with the pulse pattern electronics, dc parametric analyzer, high-speed scope, and software to enable control of the nanoprober tips and execution of the dc and pulse tests through one operator interface.

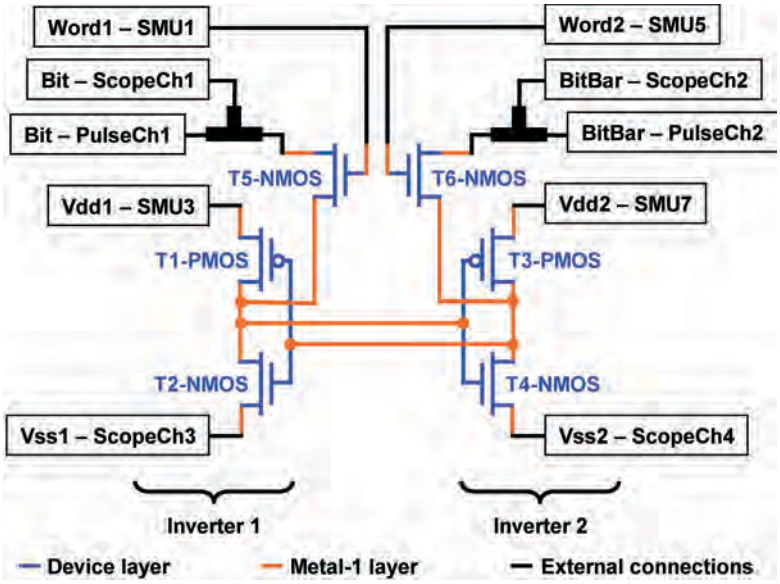

Fig. 2 *Schematic showing the six-transistor bit cell and probe and channel assignments. The blue device layer indicates the transistors and their tungsten contact-level connections. The orange metal 1 layer indicates the copper metallization layer that connects the six transistors as the two cross-coupled inverters that form the SRAM bit cell. The black lines indicate the electrical paths from the nanoprobe tips contacting the metal 1 layer in the SEM vacuum out to the test equipment.*

Data Collection and Test Description

The schematic shown in Fig. 2 describes the SRAM transistors, their metal 1 interconnections, and functional connections between the tested SRAM and the external test equipment. The dc voltage ramp graph of bit and bitbar is shown in Fig. 3(a). The high-speed corollary, the voltage pulse pattern on bit and bitbar, is shown in Fig. 4(a). The same functions of write and read are present in both versions. The dc reaction of the bit cell is shown in Fig. 3(b), and its high-speed corollary is shown in Fig. 4(b). Functionality of the bit cell is equivalently observed using both methods. It is also noted that the recorded dc bit cell reaction current matches well with the recorded high-speed values. The major differences between the dc test and the high-speed pulse test are rising and falling edges and repetition rate. The pulse test used in these measurements has 10 ns rising and falling edges and 100 ns wide write and read functions. Total duration of the pulsed test is approximately 500 ns. The pulsed test was designed to be independent of duty cycle, so that the pulsed waveform is complete with write "0" and write "1" state transitions and read functions (I_{read}) after each state change. In addition, the tested bit starts and ends in the same state. Both bit and bitbar pulse

(continued on page 26)

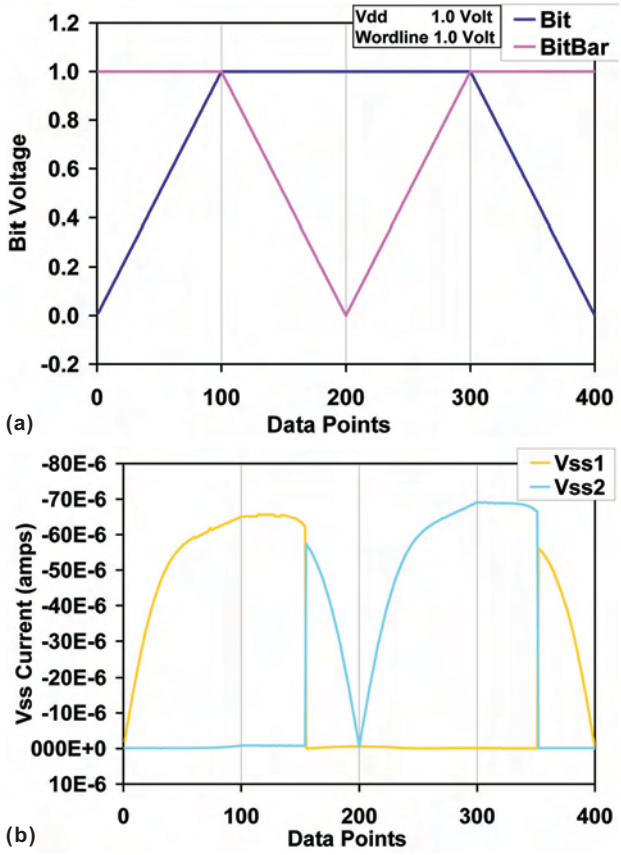

Fig. 3 *The dc bit cell stability test. (a) The dc voltage ramp of bit and bitbar connections and the dc values for V_{dd} and wordline. (b) V_{ss1} and V_{ss2} current showing the reaction of the bit cell*

(continued from page 23)

signals can only reach the SRAM inverters when wordline 1 and wordline 2 are high. This opens the channels of T5 and T6 shown in Fig. 2.

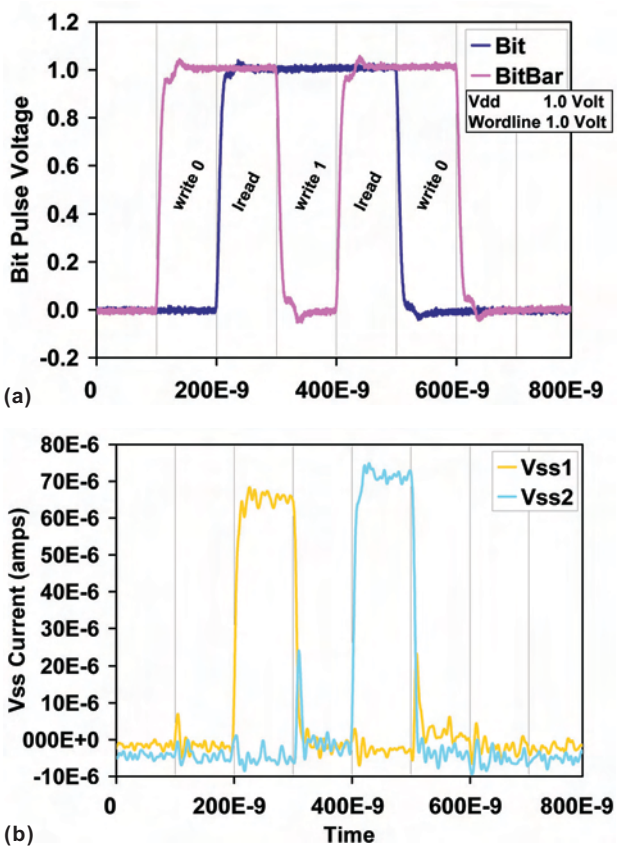

Fig. 4 *High-speed pulse bit cell stability test. (a) Voltage pulse pattern for the bit and bitbar connections with 10 ns rise and fall times with the read and write functions 100 ns wide and the dc values of V_{dd} and wordline. (b) High-speed scope capture of the V_{ss1} and V_{ss2} current showing the bit's reaction to the fast pulses and revealing the I_{read} values that were used to determine if a write function was successful*

The I_{read} function is active when both bit and bitbar are simultaneously at 1 V. The recorded V_{ss1} and V_{ss2} currents will then indicate the bit state. For example, if inverter 1 is in state "1" and inverter 2 is in state "0," then the current from the applied voltage at the bit connection will drain through T2 of inverter 1 and into the V_{ss1} connection. This will be recorded by the scope as a current pulse. Under this same state, current from the simultaneously applied voltage at the bitbar connection cannot pass through T4 of inverter 2. Thus, if inverter 1 is in state "1," then the V_{ss1} current will be high and the V_{ss2} current will be low. The exact opposite will occur if inverter 1 is in state "0"; the V_{ss1} current will be low and the V_{ss2} current will be high.

Results and Discussion

It can be difficult to isolate the single slightly out-of-specification, failure-causing transistor out of the six in a bit cell.[1] Rapid in-die bit cell fault isolation can be achieved with high-speed cycles of the bit cell stability test and simultaneous dc sweeping of the two V_{dd} connections. The high-speed waveform on bit and bitbar of the pulsed bit cell stability test consists of a sequence of write (logic 0), I_{read}, write (logic 1), and I_{read}. The 500 ns wide waveform described above can be repeated rapidly from 20 Hz to 2 MHz, depending on the desired off time or rest time of the bit cell. The two V_{dd} lines are swept down from 1 to 0 V, and the bit and bitbar connections receive the pulse pattern. The reaction of the bit cell is transmitted by the V_{ss} lines to the high-speed scope, where each reaction to the waveform is recorded. A healthy bit will eventually fault as the V_{dd} voltage drops below a certain threshold. The threshold value will be contingent on the technology being tested. A bit known to have a failure because of parametric mismatch will usually operate with nominal V_{dd} voltage, but as the V_{dd} voltage drops, the bit will fault sooner or at a higher voltage than a healthy bit.

The fault can be located by analysis of the recorded high-speed V_{ss1} and V_{ss2} currents. These currents are captured with the 5 GHz scope sample rate. This rate displays a near-continuous look at the transitions from the 0 state to the 1 state and back again. With this information, the absence of transition from one state to the other will help pinpoint the faulty SRAM inverter. Table 1 lists all of the fault possibilities, given that only one transistor of the six is the source of the fault. The column titled "Fault state" refers to the fault in transitioning from one state to the complementary state. In other words, the state listed in this column is the state in which the bit is "stuck" so that it cannot transition to the complementary state. The columns titled "Inverter 1 weak I_{read}" and "Inverter 2 weak I_{read}"

Table 1 Bit cell fail state

Faulty device low I_{dsat}(a)	Fault state(b)	Inverter 1 weak I_{read}(c)	Inverter 2 weak I_{read}(c)	State number
T1	1	F	F	1
T2	0	T	F	2
T3	0	F	F	3
T4	1	F	T	4
T5	1	T	F	5
T6	0	F	T	6

(a) T1 through T6 signify the six transistors of the bit cell under test. (b) The fault state is the condition where the bit cannot transition from one state to the complementary state. (c) The weak I_{read} columns list the true (T) or false (F) condition that an inverter's read current is 10% lower than the other inverter's read current.

indicate that the inverter 1 or inverter 2 current is 10% less than the inverter 2 or inverter 1 I_{read} current, respectively. For example, fail "State number" 2 is where the bit cannot transition from a "0" state to a "1" state, and inverter 1 I_{read} current is weaker than inverter 2 I_{read} current. Fail state 2 indicates the T2 transistor shown in Fig. 2 is the faulty device in the bit because of low drain-source saturation current. The "State number" column lists a unique state depending on which transistor is failing.

Summary

Nanoprobing used for semiconductor failure analysis does not have to be restricted only to dc or slowly varying signals. With appropriate equipment, pulses with rise and fall times as short as 10 ns can be routinely used to characterize in-die SRAM devices. Nanoprober developments in the near future will lead to improved pulse rise times as well. Fault localization of 6T SRAM bit cells can be achieved rapidly by connecting to the failing bit at the metal 1 layer. The bit's reaction can be captured in the form of fast analog current measurements, giving a unique signature of the failure. Compared to conventional nanoprobing, this test procedure can localize the failing transistor with fewer tests, decreased deprocessing need, and less posttest analysis time.

References

1. L. Liu, Y. Wang, H. Edwards, D. Sekel, and D. Corum: "Combination of SCM/SSRM Analysis and Nanoprobing Technique for Soft Single Bit Failure Analysis," *Int. Symp. Test. and Failure Analysis (ISTFA),* 2004, pp. 38-41.
2. C.M. Shen, T.C. Chuang, J.F. Chang, and J.H. Chou: "Combine Nano-Probing Technique with Difference Analysis to Identify Non-Visual Failures," *Int. Symp. Test. and Failure Analysis (ISTFA),* 2006, pp. 264-67.
3. C.P. Lin, C.H. Tang, C.H. Wu, and C.C. Ting: "Nano-Probing Application on Characterization of 6T-SRAM Single Bit Failures with Different Gox Breakdown Defect," *Int. Symp. Test. and Failure Analysis (ISTFA),* 2006, pp. 517-20.
4. R. Stallcup, Z. Cross, K. Inoue, W. James, and P. Ngo: "Bit Cell Stability Testing Using an Encoded 8 Positioner SEM Nanoprobing System," *LSI Test. Symp.,* 2007, pp. 281-86.
5. H.S. Lin and C.M. Chen: "An Application of a Nanoprobe Technique in the Characterization of Advanced SRAM Devices," *Int. Symp. Test. and Failure Analysis (ISTFA),* 2008, pp. 417-22.
6. K.A. Jenkins, J.Y.C. Sun, and J. Gautier: "Characteristics of SOI FETs Under Pulsed Conditions," *IEEE Trans. Electron Devices,* 1997, *44*(11), pp. 1923-30.
7. "Model 4200 Pulse IV Measurements for CMOS Transistors," Keithley Instruments, App. Note, 2006, PA-934 Rev. A.
8. P. Hulbert: "Dual Channel Pulse Testing Simplifies RF Transistor Characterization," Keithley Instruments, App. Note, 2008.

About the Authors

Richard Stallcup received his Ph.D. in physics with a focus on ultrahigh-vacuum (UHV) scanning tunneling microscopy (STM) from the University of North Texas in May 2000. After graduating, he received a postdoctoral position at Zyvex Corporation, where he continued to work on UHV STM systems that focused on imaging and manipulation of the atomic surface of silicon. He is now a senior scientist and the applications development manager for Zyvex Instruments, where he applies his extensive experience in atomic and molecular imaging, nanoparticle imaging and manipulation, and electrical probing at the nanoscale. Richard and his group have developed a multitude of nanoprobing applications, and they are currently focused on semiconductor FA techniques that help overcome issues with technologies below 100 nm. Richard, who is an active member of EDFAS, regularly presents his work at ISTFA.

Kanzan Inoue joined Zyvex Instruments in 2006 after a year's appointment as a postdoctoral fellow in solid-state physics with a focus on organic solar cell research at the Alan G. MacDiarmid NanoTech Institute at the University of Texas at Dallas. At Zyvex Instruments, he has been an applications development scientist, and he is involved with detailed nanoscale electrical and mechanical analysis of many new nanomaterials using Zyvex's nanoprobing systems. In addition, Dr. Inoue has developed and contributed to several key applications of Zyvex's technology, including integration into the Zyvex nanoprober system of a force-sensing cantilever that can measure nanoscale forces. His latest project has been to develop atto-Farad-scale capacitance-voltage analysis of integrated circuits using the Zyvex nanoprobing system.